RTS Amplitude Distribution in 20nm SOI FinFETs subject to Statistical Variability

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Outline

- Introduction
- Single-charge trapping in 3D tri-gate FinFETs
- Trapping interacting with variability sources
  - LER (FER & GER)
  - MGG
  - RDD
- Statistical variability dependence of RTS amplitude distribution
- $\Delta V_G - V_G$ characteristics subject to variability
- Summary
Introduction

- Why this study?
- Novel 3-D architecture FinFET is being introduced at 22nm node, with reduced variability on SOI substrate due to tolerance to low channel doping.
- But, statistical aspect of trapped charges add the statistical variability (SV) with stress time.
- On nanoscale, interactions of trapping with SV sources are complicated, which greatly alter the understanding and behavior of BTI.
- BTI behavior is a manifestation of multiple trapping. Understanding RTS behavior is a bridge to understand BTI through trapping probability distribution.
FinFET

Fin Edge Roughness: width, height, slope

Bulk substrate

SOI substrate

Intel 22nm

IMEC Veloso et. IEDM, 2009

TSMC Chang et., IEDM, 2009

IBM Chang et., VLSI tech., 2011
Simulation Design of FinFETs

Tri-gate SOI FinFET

0.005 acceptor in channel

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lg (nm)</td>
<td>20</td>
</tr>
<tr>
<td>EOT (nm)</td>
<td>0.83</td>
</tr>
<tr>
<td>Wfin (nm)</td>
<td>10</td>
</tr>
<tr>
<td>Hfin (nm)</td>
<td>25</td>
</tr>
<tr>
<td>Nsd (cm⁻³)</td>
<td>3.0E20</td>
</tr>
<tr>
<td>Nch (cm⁻³)</td>
<td>1.0E15</td>
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<tr>
<td>Vdd (V)</td>
<td>1.0</td>
</tr>
<tr>
<td>Ioff (nA/µm)</td>
<td>97</td>
</tr>
<tr>
<td>Idsat (µA/µm)</td>
<td>1411</td>
</tr>
<tr>
<td>SS (mV/Dec)</td>
<td>76.8</td>
</tr>
<tr>
<td>DIBL (mV/V)</td>
<td>46.7</td>
</tr>
</tbody>
</table>

Ref.: ITRS 2010 update

Wang et al., IEDM 2011, p5.4.1
Single trapped charge

- Trapped charge induces Coulomb potential peak.
- It can block the nearby current.
- Radius $\approx 3\text{nm}$ at subthreshold. It depends on gate bias.
Intrinsic Parameter Fluctuations
Statistical Variability

Random dopants
Polysilicon/Metal Gate Granularity
Line Edge Roughness
Reported $V_T$-shift measurement

Bulk planar transistor, $V_T$-shift steps with relaxation.

1) Exponential; 2) Large $V_T$-shift is caused by trapped charge interaction with current percolation path, which formed by RDD in bulk conventional transistors

Franco, Kaczer, et al., 2012 IRPS
Simulation: Conventional Bulk MOSFET (STMicroelectronics 32/28nm node)

- Close to exponential;
- Large $V_T$-shift tail is created by interaction of trapping with RDD induced percolation.
RTS amplitude distribution in FinFETs

- Upper bounded in uniform device.
- Extended tail in ‘atomistic’ devices.

Charge is trapped:
- at narrowing fin;
- under a metal grain with low-WF.

FER, MGG, RDD.

X. Wang, et al., SNW 2012
Interaction with LER (FER and GER) induced crowded current path

- Narrow regions of fin leads to the crowded current, which is sensitive to charge-trapping blocking effect. Similarly, local short-channel regions are also susceptible.
Interaction with MGG induced potential barrier variation

- Low potential barrier region holds the large current density.
Interaction with RDD induced percolation path

- Number of Acceptors $\sim N_{ch} \times (L_G \times W_{fin} \times H_{fin})$ Poisson
  e.g. $N_{ch}=5E17\text{cm}^{-3}$, 2.5 acceptors in average
- Acceptors in the upper channel create the percolation path at the bottom
• Basically, the average RTS amplitude increases with larger statistical variability magnitude.
• It has the largest dependence on RDD induced variability.
• Only modeling charge trapping is physically not enough!
The standard deviation of $\Delta V_T$ is also dependent on statistical variability source and statistical variability magnitude.

- It has the largest dependence on RDD induced variability.

1.2 charges in average
\( \Delta V_G - V_G \) characteristics

- \( \Delta V_G \) is the fractional gate-voltage required for single-charge trapped FinFETs to have the same drain-current with fresh device.
- The magnitude show large variation, increasing or decreasing locally.
- Challenge for compact modelling.
The distribution of the fractional gate-voltage needed to have the required drive current.

- Vary with different variability sources.
Summary

• RTS amplitude is affected by charge trapping location, and underlying irregular current flows induced by statistical variability (SV) sources.

• (1) Same as in bulk planar transistors, current percolation created by RDD is sensitive to proximate charge trapping; (2) LER (FER & GER) shapes the local narrow/short channel regions, which are also susceptible to charge trapping; (3) Local low channel potential barrier regions from WFV in MGG holds large current therefore leads to large $V_T$ RTS shift.

• RTS amplitude distribution in SOI FinFETs deviates from exponential due to SV reduction, and its average and standard deviation depends on SV magnitude.

• $\Delta V_G - V_G$ characteristics demonstrate significant variation in magnitude and trends, giving a big challenge to compact modelling.
Acknowledge

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• Thank you for your attention.