Electronic Systems Design 3 – Dummy Exam Paper

The degree exam paper will have a front page with the information contained in the box below. Section A will contain three, 20 mark questions on the analogue side of the course. Section B will contain three 20 mark questions on the digital side of the course. The questions contained in this dummy paper should be at approximately the level of difficulty to be expected in the degree exam. Of course it is impossible to cover all the examinable material from the course in a single dummy paper, so be careful to also revise those areas of the course which, although not in this paper, seem ripe for exam questions!

Note: Unlike exams you may have taken last year, *no crib sheet* of VHDL examples will be provided. You are expected to have a working knowledge of the VHDL language. However you will not be expected to write perfect VHDL from 'cold'. You will be expected to be able to substantially alter or augment an existing code example, or complete unfinished code. Marks will not be deducted for trivial errors in VHDL syntax.

Monday 4th June 2001
9:30 – 11:30 a.m.

ELECTRONIC SYSTEMS DESIGN 3

Answer **4 (four)** questions from Section A and Section B

The numbers in square brackets in the right-hand margin indicate the marks allotted to the part of the question against which the mark is shown. These marks are for guidance only.

Q1. (a) Draw the equivalent circuit diagram of an opamp showing sources representing input offset voltage and input bias currents.

[4]

(b) Explain why it is often helpful to represent bias currents flowing into the opamp inputs as offset and bias currents, and distinguish between the two.

[3]

(c) A noninverting amplifier is required to condition the output of a thermocouple temperature sensor having the following properties:

Resistance $10\text{k}\Omega$
Sensitivity $150\mu\text{V}\cdot\text{K}^{-1}$

If the output of the amplifier is to have a sensitivity of $20\text{mV}\cdot\text{K}^{-1}$ design the amplifier.

[3]

(d) For your amplifier calculate the DC output error due to offset current, offset voltage and, if relevant, bias current.

[7]

(e) Hence define a figure of merit which represents the quality of the opamp used in your circuit.

[3]

Q2. (a) Figure Q2a) shows the circuit diagram of an amplifier. Derive an expression for the output as a function of input assuming that R1 = R2 and R3 ≈ R4 such that R3=R4+Δ, where Δ is small relative to R3,4. [6]

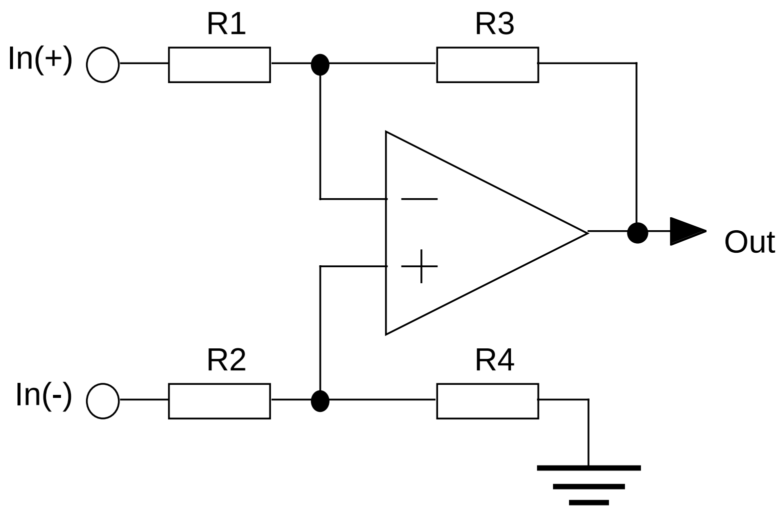


Figure Q2a)

(b) Hence calculate the differential and common-mode gains of the amplifier. [2]

(c) Draw the circuit diagram of a classical 3-opamp instrumentation amplifer. [2]

(d) Without further calculation write down an expression for the common-mode and differential gain of the complete amplifier. [2]

(e) An instrumentation amplifier is required to condition the output of a resistance bridge as shown in figure Q2e). If R* = R±0.01%. Calculate the CMRR required to detect the change in R*. [5]

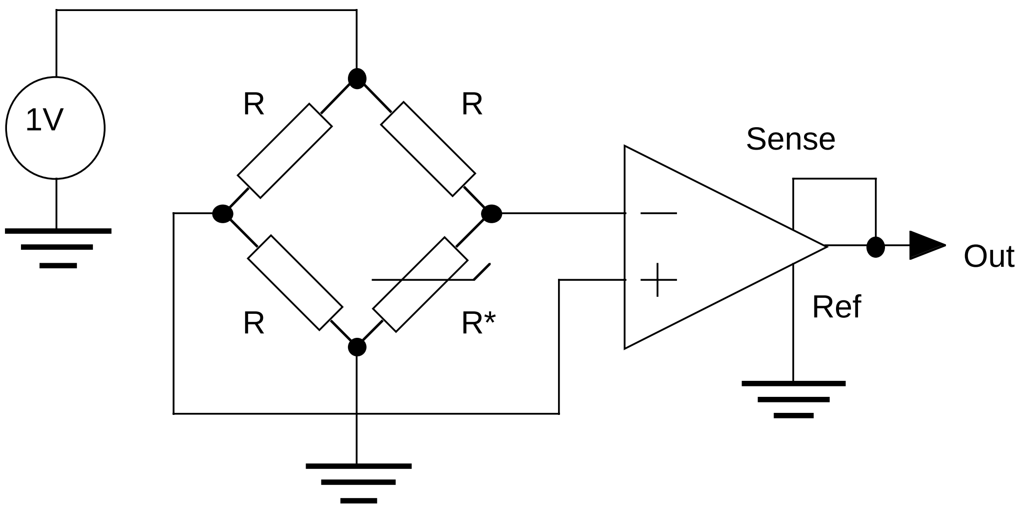


Figure Q2e)

(f) If the resistors in figure Q2a) have a tolerance of 1%, what is the minimum gain which can be used to meet the CMRR specification? [3]

Q3. Figure Q3 shows the circuit diagram of a low noise amplifier constructed using an operational amplifier used to measure the voltage generated by a resistive source, represented by the combination R_S and V_S in the figure.

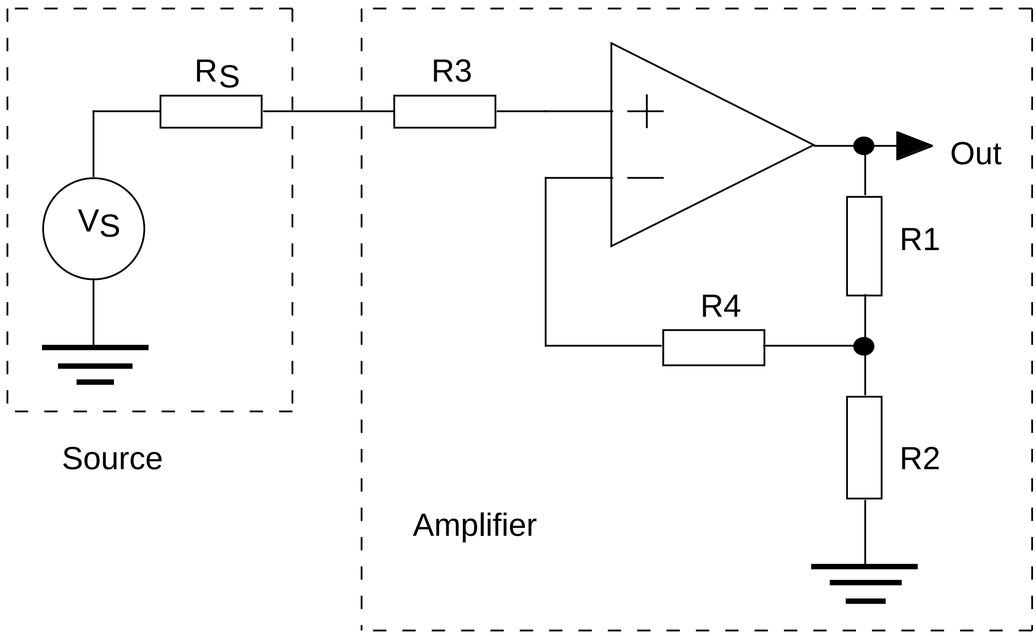


Figure Q3

Component values are :
R1 = 50Ω   R2 = 4950Ω   R3 = 100Ω   R4 = 20kΩ R_S = 20kΩ

(a) What is the purpose of R4? [2]

(b) Re-draw the amplifier circuit diagram incorporating all noise sources. [6]

(c) Calculate the thermal noise voltage spectral density present in the source resistor. [2]

(d) If the input voltage noise of the amplifier is $V_n = 20nV \cdot Hz^{-1/2}$ and the input current noise of the amplifier is $i_n = 0.91pA \cdot Hz^{-1/2}$ calculate the total input equivalent noise voltage at a temperature of 300K [4]

(e) Hence calculate the noise figure of the amplifier. [2]

(f) What is the noise figure of the amplifier if the temperature of the source resistor (but not the other components) is reduced to 100K? [4]

Note: The voltage noise spectral density of the thermal (Johnson) noise of a resistor is given by

$V_{Th} = \sqrt{4k_B TR}$ where

k_B is Boltzmann's constant, $1.38 \cdot 10^{-23} J \cdot K^{-1}$
T is the temperature in Kelvin
R is the resistance in Ohms

OVER

Q4. (a) Describe how a linear feedback shift register might be used in the process of data encryption and decryption. Give three properties of linear feedback shift registers which make them useful for such a task, indicating the reasons why these properties are important.

[5]

(c) What is the maximal length of bit pattern associated with a 5-bit linear feedback shift register? By writing down the characteristic polynomial of the shift register of figure Q4a and showing it to be non-primitive (or by any other means), prove that the system of Figure Q4a does not have maximal length.

[7]

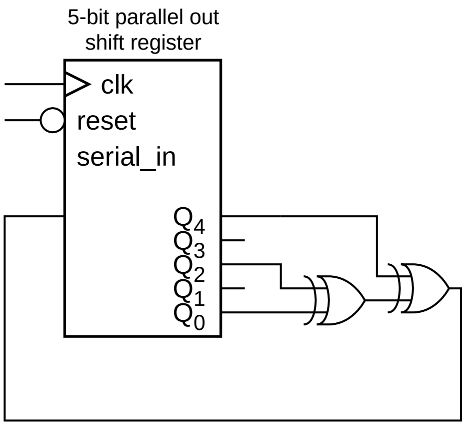


Figure Q4a

(d) Using the data given in figure Q4b, draw a maximal length 5-bit linear feedback shift register which uses two exclusive-or gates. How many such registers are possible?

[5]

Degree	Primitive Polynomials Modulo 2*
1	0 (i.e., $x + 1$)
2	1 (i.e., $x^2 + x + 1$)
3	1, 2 (i.e., $x^3 + x + 1$ and $x^3 + x^2 + 1$)
4	1, 4 (i.e., $x^4 + x + 1$ and $x^4 + x^3 + 1$)
5	2, 4, 7, 11, 13, 14
6	1, 13, 16, 19, 22, 25
7	1, 4, 7, 8, 14, 19, 21, 28, 31, 32, 37, 41, 42, 50, 55, 56, 59, 62
8	14, 21, 22, 38, 47, 49, 50, 52, 56, 67, 70, 84, 97, 103, 115, 122

*Expressed as a decimal integer representing the interior bits (that is, omitting the high-order bit and the unit bit).

Figure Q4b

(e) Modify your maximal length 5-bit linear feedback shift register with the additional logic necessary for it to pass through *all* 5-bit states including "00000".

[3]

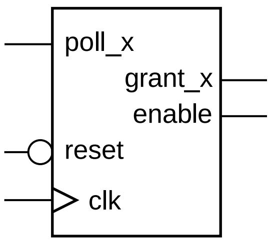
OVER

Q5. (a) Name two common hardware description languages and discuss how such languages enhance the process of digital design.

[5]

(b) Figure Q5a shows the inputs and outputs to a simple controller system designed to control access to a databus for a device *x*. The VHDL architecture for the controller is also given. The system monitors `poll_x` until it becomes active at which point `grant_x` is made active and `enable` raised. Given a supply of D-type edge triggered flip-flops and two input AND gates, how many would be needed to realise this design in hardware ?

[5]




```
architecture behavior of handshaker is
   type state is (poll, grant);
   signal present_state, next_state : state;
begin

   process(clk)
   begin
      if clk'event and clk='1' then
         if (reset='0') then
            present_state <= poll_x;
         else
            present_state <= next_state;
         end if;
      end if;
   end process;

   process(present_state, poll_x)
   begin
      grant_x <= '0'; enable <= '0';
      next_state <= poll;
      case present_state is

         when grant =>
            grant_x <= '1'; enable <= '1';
            if (poll_x='1') then
               next_state <= grant;
            else
               next_state <= poll;
            end if;

         when poll    =>
            grant_x <= '0'; enable <= '0';
            if (poll_x='1') then
               next_state <= grant;
            else
               next_state <= poll;
            end if;

         when others  =>
      end case;
   end process;
end behavior;
```

Figure Q5a

(c) Write VHDL architecture code for the more complex controller shown in figure Q5b. Two competing devices *x* and *y* wish access to the bus by raising `poll_x` or `poll_y` respectively. Device *x* should always be given priority over device *y*, and whenever either of them is granted access to the bus, `enable` should be raised along with the appropriate `grant` signal. The controller reset should be asynchronous active low.

[10]

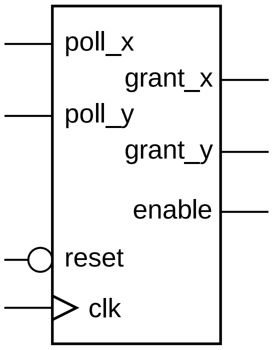


Figure Q5b

Q6. (a)Consider the diagrams of figure Q6a, which show the structure of a static RAM module and associated read timing. State the size of this memory (both number of words and word length).

[2]

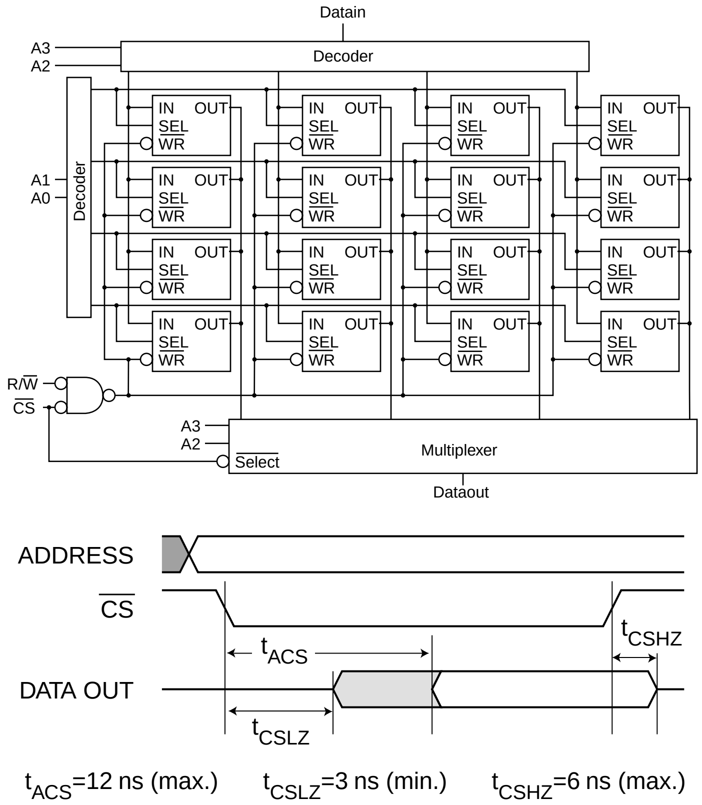


Figure Q6a

(b) This memory is uses as part of a synchronous system, with inputs being fed directly from the outputs of registers with t_{pd} = 5 ns (rising clock edge to stable output) and output *Dataout* being fed to a register with setup and hold times of t_s = 3ns and t_h = 2ns respectively. What is the maximum clock frequency of this system which avoids the possibility of metastability.

[5]

(c) Design and sketch a 32 word memory using the modules of figure Q6a where each word is 2 bits wide. (Do not attempt to redraw the internal structure of each module, simply use an outline box for each one with the inputs and outputs shown). Describe any additional logic components used.

[5]

(d) Describe the underlying physical processes which allow data storage in both DRAM and SRAM memories. Hard Disk manufacturers often design systems containing cache memory for temporary storage of data which has not been requested by the CPU on the assumption that the data *will* be needed shortly. Discuss the advantages and disadvantages of DRAM and SRAM for this application.

[8]

END