Dummy Exam 2004/05 Session

University of Glasgow

DEGREE OF MASTER OF ENGINEERING (M.Eng.)

DEGREE OF BACHELOR OF ENGINEERING (B.Eng.)

DEGREE OF BACHELOR OF SCIENCE (B.Sc.) IN ENGINEERING

ANALOGUE ELECTRONICS (AERO)

Answer all questions.

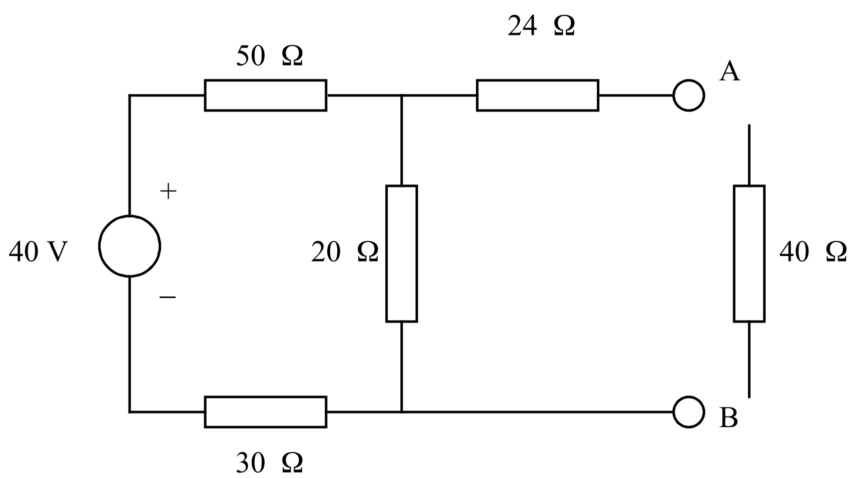
The numbers in square brackets in the right-hand margin indicate the marks allotted to the part of the question against which the mark is shown. These marks are for guidance only.

If an electronic calculator is used, intermediate steps in the calculation should be indicated.

Q1 (a) Show that the Thévenin equivalent of the circuit in figure below is an 8 V source in series with a 40 Ω resistor. [8]

(b) Calculate the power which would be dissipated in a 40 Ω resistor connected between the terminals A and B. [3]

(c) Calculate the maximum and minimum resistances which might be substituted for the 40 Ω resistor and still give a power dissipation of at least 75% of the maximum value. [9]

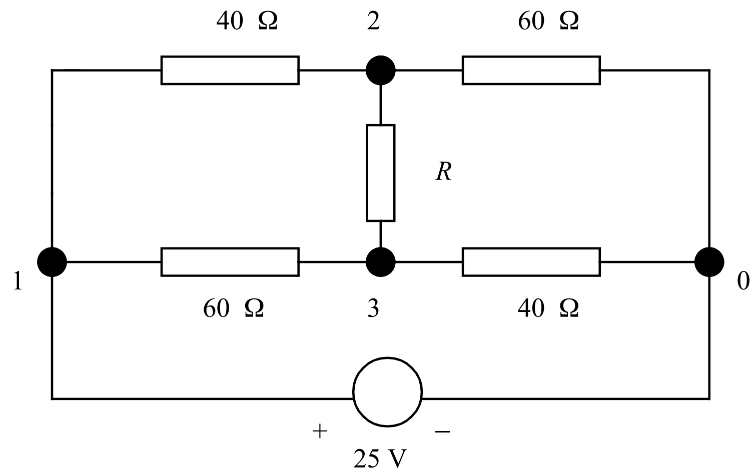


OVER

Q2 (a) For the circuit shown below, use nodal analysis to write down the current balance equations at nodes 2 and 3 in terms of V_2, V_3 and R. V_2 and V_3 are respectively the voltages at nodes 2 and 3 relative to the voltage at node 0, which is assumed to be 0 V. [8]

(b) If the voltage at node 2 is 1 V higher than the voltage at node 3, calculate the values of V_2, V_3 and R. [6]

(c) Hence determine the current supplied by the 25 V source and the equivalent resistance of the network of resistors when the voltage at node 2 is 1 V higher than the voltage at node 3. Compare this resistance with the values for the network resistors when $R \to 0$ and $R \to \infty$ [6]



OVER

Q3 An a.c. supply of amplitude 20 V and of frequency 5 kHz is connected across a resistor $R = 4.7\ \text{k}\Omega$ and a capacitor $C = 10\ \text{nF}$ (10×10^{-9} F) connected in series. See the diagram below. If the output resistance of the voltage source, R_S, is assumed initially to be 0 Ω, find:

(a) the impedance of the circuit in both $R + \text{j}\,X$ and $Z\angle\phi$ form, [4]

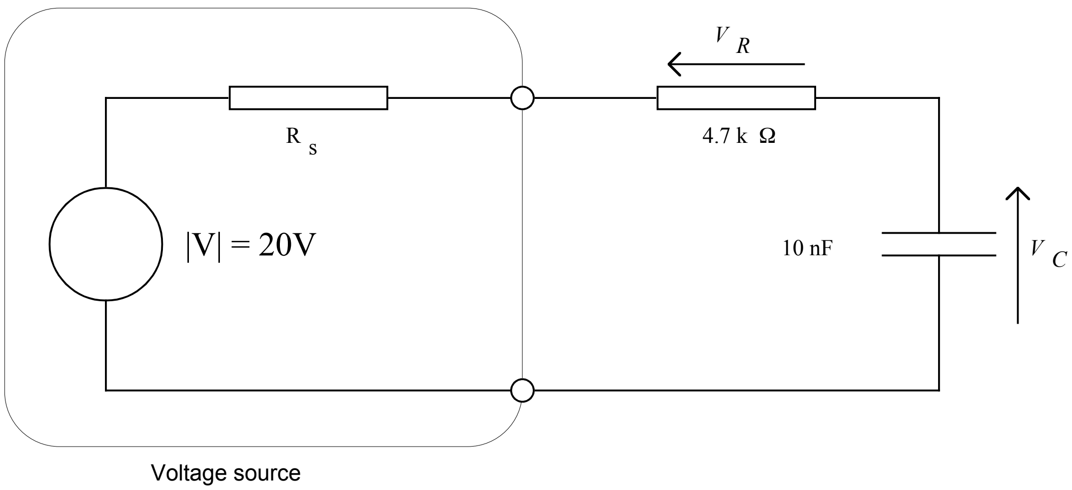
(b) the magnitude of the current flowing in the circuit, [2]

(c) the phase difference between the applied voltage and the current, and [2]

(d) the voltage across the resistor and the voltage across the capacitor. [2]

(e) Show that $V_R + V_C$ is equal to the voltage applied to the circuit. [4]

(f) It is suspected that R_S, the output resistance of the voltage source, is not actually 0 Ω. When the circuit is investigated experimentally, it is found that the phase difference between the applied voltage and the current is actually 31°. From this observation calculate R_S [4]

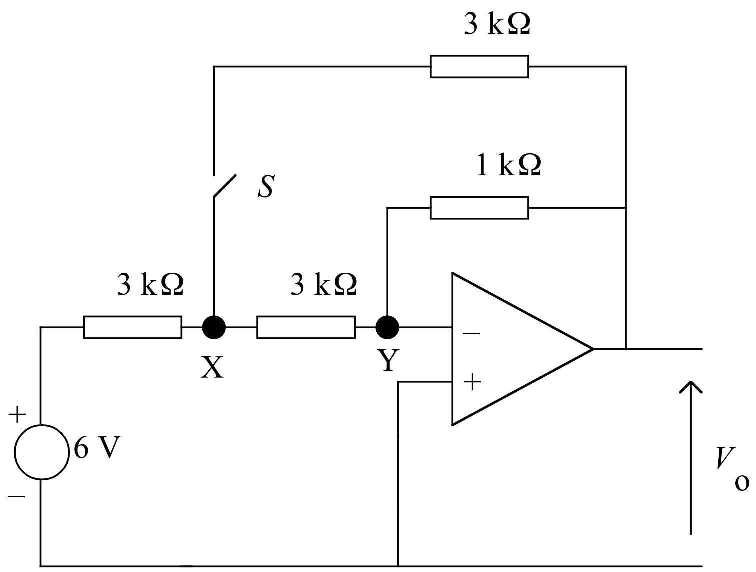


OVER

Q4 (a) What assumptions can be made about an op-amp which is described as being ideal ? [4]

(b) The op-amp shown below can be assumed to behave in an ideal fashion. In the voltage reduction circuit shown in the diagram the switch *S* is initially open. Calculate the output voltage V_o. [6]

(c) The switch *S* is now closed. Use nodal analysis at nodes X and Y to determine V_x and then calculate V_o. [10]



END