Following their invention in 1947 at Bell Laboratories\textsuperscript{1} [1.1], transistors have since dominated the semiconductor market as the main component of electronic circuits. It is not an exaggeration to claim that the introduction of the transistor to electronic circuits allowed today’s microelectronics systems, computer technology, telecommunications, space exploration, and modern scientific research in general [1.2].

About a decade following the invention of the transistor, the development of integrated circuits (IC) opened up a new era for transistor applications in electronic circuits [1.3] [1.4] [1.5]. Since the first ICs, the market has continued to demand greater and greater functionality per package component. Industry is striving to satiate this demand by increasing the number of transistors on a chip. Naturally, however, at the same time industry insists on keeping the cost of production to a minimum.

The scaling down of transistors is widely regarded as the best way to meet the growing demand for a high volume of transistors integrated into a single chip. The idea of scaling conventional transistors [1.6], which is the main theme of this research, then gathered apace to revolutionize the advancement of the microelectronics industry.

This introduction discusses the motivation, problems and main objectives of the research presented in the thesis. It also outlines the overall structure of the thesis.

\textsuperscript{1} Three scientists, William Shockley, Walter Brattain and John Bardeen, are credited for the invention of the transistor at Bell Laboratory in 1945 and all three received Nobel price for their contribution to physics.
1.1 Motivation and description of the problems

One of the important growth drivers for the semiconductor industry is the shrinking of transistors to smaller dimensions. The reduction of transistor size increases performance. System performance and functionality increases as the density of transistors which can be integrated onto a single chip increases. At the same time switching speed increases inversely proportionally with gate length ($L_g$), allowing faster circuit operation [1.7]. Another benefit of scaling transistors is the reduction in manufacturing costs per device.

Despite the challenges and difficulties regarding MOSFET miniaturisation, scaling still continues to dominate semiconductor research and development programmes. However, problems limiting the scaling of conventional MOSFETs continue to challenge. These limitations and the corresponding technological challenges are currently dictating a shift of research from conventional MOSFET to alternative devices.

According to the International Technology Roadmap for Semiconductors (ITRS), if Moore’s law [1.8] is maintained the microelectronics industry expects the mass production of 7 nm physical gate length transistors in twelve to fifteen years’ time. Realization of such atomic scale transistors is technologically challenging, if not unattainable. To reach this level of miniaturisation will require an enormous amount of research and resources. So far, the semiconductor industry has pursued a traditional performance trajectory [1.9]. However, keeping to this tradition by using conventional ways of scaling is a monumental task as we approach ‘decananometre’ (tens of nanometres) channel devices.

Unfortunately, the scaling of conventional MOSFETs is fast approaching its zenith [1.10]; there are some fundamental physical and material limitations that hinder the progress of scaling. Some of these fundamental problems are, for example: short channel effects, unacceptably high off-state currents which induce a high (static) power dissipation, lack of performance and intrinsic parameter fluctuations. The challenges of keeping to the present scaling trends for conventional MOSFETs and the increasing interest in alternative transistor architectures are the main motivations of this research work.
1.2 Research objectives

The first major objective of this research is by using commercial process and device Technology Computer Aided Design (TCAD) tools, to design well scaled conventional MOSFETs with gate lengths\(^\ddagger\) of 35, 25, 18, 13, and 9 nm, corresponding to the 90, 65, 45, 32, and 22 nm technology nodes respectively and to study in detail their electrical properties.

The scaling is based on a real state of the art 35 nm MOSFET, which has been used to guide the design of the scaled devices under study. The simulation tools have been appropriately calibrated in respect of this benchmark device. The study of the scaled devices aims to further enhance the qualitative and quantitative understanding of the main factors limiting the scaling of conventional CMOS in accordance with the requirements of the latest ITRS. A comprehensive investigation of the electrical characteristics and parameters of the scaled devices should lead to a more detailed understanding of the problems of scaling. The better understanding leads to possible solutions for the challenges which the semiconductor industry faces, up to and beyond the end of the ITRS in 2018. This work also tries to contribute answers to common questions asked by researchers and technologists, such as: “are we near the end of the ‘classic’ scaling pattern? When will it end and how? Can we go beyond ITRS’s present predictions of scaling? Do we really need new device architectures? If so how far can we go with them?”

The second major objective of this research is to investigate how far intrinsic parameter fluctuations affect the characteristics and the integration of the advanced MOSFETs. This was done by employing 3-D atomistic device simulation software

\(^\ddagger\) It is important to note that the gate length mentioned above and frequently used throughout this thesis correspond to the “physical gate” length rather than the “printed gate” lengths or channel length (effective channel length). According to the definitions given in the latest ITRS 2003 edition, printed gate length refers to the requirements by the semiconductor industry “as-printed” in photo resist prior to etching. On the other hand, the physical gate length (“as etched in polysilicon”) may be reduced from the “as-printed” dimension as a result of etching process. Since this work is mainly interested on high performance devices which derive the miniaturization of transistors, the physical gate length has been considered as a minimum feature size during the scaling.
developed by the Device Modelling Group at the University of Glasgow. In essence, one is trying to answer the following questions: How can the effects of fluctuations be suppressed and by what means? Can we predict the extent to which intrinsic fluctuations hamper the progress of conventional MOSFET scaling? Based on the analysis of the information and data obtained from computer simulation and experimental results, an attempt has been made to find solutions to circumvent these problems.

1.2 Thesis outline

The thesis is divided into seven chapters of which three chapters (chapters 4, 5, and 6) contain simulation results and discussions. Chapters 2 and 3 contain back-ground information and a description of the simulation methodology developed and used to perform the research task. In the following sections, a condensed summary of each chapter is given.

Chapter 2 introduces Moore’s law, the International Technology Roadmap for Semiconductors (ITRS) [1.12] and the scaling concepts of conventional MOSFETs. The emphasis is placed on the projected miniaturisation of MOSFETs according to the requirements and the technology nodes of the present ITRS edition. The chapter starts by reviewing Moore’s law from a historical and economic perspective and its contribution to the advancement of the semiconductor industry. The discussion expands to the driving role of the ITRS in relation to device scaling and the complimentary relationships between Moore’s law and the ITRS.

The two main approaches to scaling are then described, namely the constant field scaling and the generalised scaling rules. The fundamental limitations to conventional MOSFET scaling are also discussed in conjunction with these two approaches. The final section of Chapter 2 gives historical insights into the evolutionary development of field effect transistors (FETs) and looks at possible future directions, through a review of the present state of MOSFETs and the semiconductor industry.

Chapter 3 focuses mainly on the methods employed in this research. This includes the systematic calibration, simulation, modelling, and scaling of conventional MOSFET devices. The process and device simulation techniques, which have been used
to calibrate and simulate the Toshiba 35 nm MOSFET, are explained in detail. The different models employed and their specific parameters are explained in detail.

The results and discussions on the calibration, scaling and simulation of the scaled devices are presented in chapter four. The device structures of both the *n* and *p*-channel real 35 nm MOSFETs are described. This is followed by a description of the structure and the comparative characterisation of the scaled devices with 25, 18, 13, and 9 nm channel lengths. Additionally, the carrier mobility in the 35 nm and scaled transistors is studied in conjunction with the electric fields and doping concentrations at the Si/SiO₂ interface.

One of the major limiting factors of conventional MOSFET scaling are the intrinsic parameter fluctuations resulting from the position and number of random discrete dopants in the active region of the transistor or from gate line edge roughness. The statistical investigation of the impact of both the discrete random dopants and gate line edge roughness on the performances of 35 nm and scaled (25, 18, 13, and 9 nm) MOSFETs are presented in chapter 5.

There is a general consensus that the scaling of conventional MOSFET is nearing its end. It is important that the semiconductor industry looks for new technologies and device architectures. One of the promising emerging devices is the Ultra Thin Body (UTB) SOI FET. In the course of this research we have investigated the electrical properties of UTB SOI FETs under different scaling scenarios, which correspond to the 32 nm and 22 nm technology nodes. Chapter 6 presents the results of the scaling of these Ultra-Thin Body SOI FETs.

Finally, Chapter 7 of this thesis presents a summary of the main findings of the PhD research. In addition to the concluding remarks some suggestions for future research work are also outlined, highlighting some of the important research areas which may offer further insight into the simulation understanding and design of decananometre MOSFETs.
1.5 Chapter references