Parameter fluctuations found in ultrasmall devices are generally associated with discrete random dopants in semiconductors [1, 2]. However, dopants are not the only source of intrinsic fluctuations in device characteristics that can impede the traditional scaling approach in sub-100 nm MOSFETs. Other stochastic effects, such as oxide thickness fluctuations, can also contribute to variations [3]. Line edge roughness (LER), which does not scale with geometry in most types of lithography processes, also introduces intrinsic parameter fluctuations and becomes of increasing concern below 100 nm, even in well-scaled devices [4].

Although several workers have investigated the impact of LER in device simulations, these attempts do not account for the true 3D statistical nature of LER. So far all modelling studies have approximated LER in a 'square-wave' fashion in deterministic simulations [5, 6] or take advantage of faster 2D device simulations in a simplistic statistical approach [7]. We approach the simulation of LER in decanano MOSFETs for the first time in a truly 3D statistical fashion. LER in our simulations is specified in terms of actual statistical parameters, i.e., rms amplitude (Δ) and correlation length (Λ). This allows both 3D and statistical aspects of LER to be naturally incorporated in a single simulation framework.

Data obtained from a variety of processes, as presented in Fig. 1, attest to a minimum total LER limit (3Δ) of 5–6 nm, which is larger than the Roadmap requirement for devices below 100 nm [4]. This alarming, especially given that metrology requirements are often more difficult to meet than actual linewidth specifications for a given process. Less is known regarding the correlation length of LER, which is reported to vary between 10 nm and 50 nm [7].

Our approach to the reconstruction of realistic gate edges is based on a 1D Fourier synthesis approach, assuming a Gaussian or exponential autocorrelation function for the LER. Random line examples generated using this approach are given in Fig. 2 for typical values of Δ and Λ. Such synthesized lines, with correct statistical properties, are used in our 3D simulations to determine source/drain junctions in ensembles of 200 MOSFETs, which have otherwise identical design parameters (Fig. 3). For the sake of simplicity and speed we use the drift-diffusion approximation, with constant mobility [12], and neither the quantum mechanical nor the atomistic doping options are enabled during simulations. A set of 200 devices takes 0.5–4 days to run on a single processor depending on the bias conditions, although in practice several processors are used in parallel. This is in marked comparison with 3 months reported for 70 MOSFETs in [7].

We study the impact of LER on MOSFETs at several nodes on the SIA roadmap for a range of Λ and Δ values. Specifically, we focus on the variation of threshold voltage, V_T, leakage current, I_{off}, and drive current, I_m. Devices considered here comply with scaling requirements at each technology node and assume a Gaussian autocorrelation for LER used to construct the source/drain junction edges.

LER causes threshold fluctuations similar to those resulting from other stochastic effects, as can be seen in Fig. 4. Fluctuations increase when rms amplitude is high or when devices are scaled down. The average value of threshold voltage is affected too, and the magnitude of the fluctuations are comparable to those reported for random dopants in similar devices [2].

Several interesting features of our simulations are presented in Fig. 5 to Fig. 8. Leakage current appears to be extremely sensitive to LER in a 30 nm MOSFET. On-current is also affected, while the ratio of their average value ∆I_m/|I_m| (not shown) increases by 66% in this device. Correlation length dependence of LER saturates at relatively low values of Δ. The current distributions disclose slight skew, which may be attributed to increased short channel effects in shorter elements of the ensemble, not to operational asymmetry between source and drain. We will demonstrate how LER may inhibit MOSFET scaling below 50 nm, unless reduced significantly both in transverse and lateral directions.

References
Figure 1: LER found in various advanced lithography systems including IBM [7], ASET [8], IMEC [9], Sandia Labs [10], SONY [11] and required by SIA roadmap [4]. The inset shows LER observed in sub-100 nm e-beam generated lines.

Figure 2: LER model used in 3D device simulations. Both the power spectra (top) and corresponding line data (bottom) are shown.

Figure 3: A typical 50×50 nm MOSFET used in 3D simulations, with LER parameters $\Lambda=10$ nm and $\Delta=3$ nm.

Figure 4: Standard deviation of threshold fluctuations in decanan MOSFETs as a function of rms fluctuations at $V_D = 1.0$ (squares) and $V_D = 0.1$ (circles) Volts. $\Lambda=20$ nm.

Figure 5: Dependence of drain current standard deviation on the LER rms amplitude for a 30×30 nm MOSFET with $\Lambda=20$ nm.

Figure 6: Dependence of drain current standard deviation on the LER correlation length for a 50×50 nm MOSFET with $\Delta=2$ nm.

Figure 7: Histograms of on-current distribution in 200 (30×30 nm) MOSFETs for three $\Lambda$ values.

Figure 8: Comparison of 50 nm device simulations with LER present only on the drain or the source side in the ensemble. Note that $\Lambda=20$ nm, $V_D = 1.0$ and $V_G = 0.0$ Volts.