Quantitative Evaluation of Statistical Variability Sources in a 45-nm Technological Node LP N-MOSFET

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***Abstract*—A quantitative evaluation of the contributions of different sources of statistical variability, including the contribution from the polysilicon gate, is provided for a low-power bulk N-MOSFET corresponding to the 45-nm technology generation. This is based on a joint study including both experimental measurements and "atomistic" simulations on the same fully calibrated device. The position of the Fermi-level pinning in the polysilicon bandgap that takes place along grain boundaries was evaluated, and polysilicon-gate-granularity contribution was compared to the contributions of other variability sources. The simulation results indicate that random discrete dopants are still the dominant intrinsic source of statistical variability, while the role of polysilicon-gate granularity is highly dependent on Fermi-level pinning position and, consequently, on the structure of the polysilicon-gate material and its deposition and annealing conditions.**

***Index Terms*—Matching, mismatch, MOSFET, parameter fluctuations, variability.**

I. Introduction

IT HAS BECOME clear that the statistical variability in the transistor characteristics will be one of the major challenges for coming technological nodes [1], [2]. The detailed knowledge of variability sources is extremely important for the design and manufacturing of variability-resistant devices. Whereas the impact of random dopants, line-edge roughness (LER), and oxide-thickness variations is relatively well understood [3], the role of the polysilicon-gate has only lately been investigated in simulations, and experimental confirmation and quantification of its contribution is still lacking. It was first shown that gate could be a significant source of variability in [4], and at that time, the observed enhanced variability was attributed to random polydepletion and boron penetration. Later, owing to grain-size reduction, spectacular variability reduction was shown in [5] and, more recently, in [6] with the usage of micrograin polysilicon. Even more recently, it was shown that amorphous-silicon gates lead to less variability, since they suppress random channeling penetration of pocket implants [7]. The impact of the Fermi-level pinning at grain interface and the corresponding threshold-voltage shift was first discussed in [8], and the dependence with both grain boundaries' interface charge density and position along the channel is further studied in [9]. Finally, based on such a model, statistical 3-D simulations confirmed the significant role of the polysilicon on the statistical-parameter variations through the random grain distribution [10]. But properly quantifying the polysilicon-gate contribution requires the detail position of the Fermi-level pinning states in the bandgap and their density, which are difficult to determine experimentally. Here, for the first time, we compare statistical 3-D simulations and experimental measurements of 45-nm n-channel MOSFETs in order to estimate the magnitude of this effect. This allowed the proper quantization of the polysilicon-gate contribution in comparison to the contributions of the other sources of variability and the determination of the likely position of the Fermi-level pinning at the polysilicon grain boundaries [13], [14].

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II. Measurements and Simulations Methodology

A. Device Description and Measurement Methodology

The n-channel MOSFET under consideration is a low-power (LP) device from the STMicroelectronics 45-nm platform with a 42-nm polygate length and a 1.7-nm oxide thickness. The device structure is shown in Fig. 1. Local fluctuations were measured on matching test structures that consist of pairs of identically designed devices, placed at quasi-minimal spacing the one from the other, and individually addressable with separated drain, source, and gate. Threshold-voltage differences ($\Delta \mathrm{Vt}$) were measured on 70 pairs, using a constant-current criterion ($I = 70$ nA $\cdot$ W/L). At a 99% confidence level and considering these 70 measured samples, the real value of $\Delta \mathrm{Vt}$ standard deviation ($\sigma \Delta \mathrm{Vt}$) is within the $[-18\%, +27\%]$ interval around its estimation.

B. Simulations Methodology

The Glasgow statistical 3-D device simulator solves the carrier-transport equations in the drift-diffusion approximation

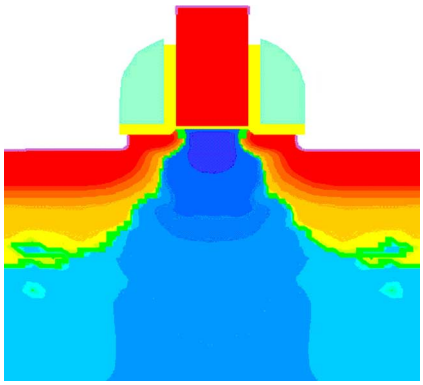

Fig. 1. Nominal-device structure and net-doping profile.

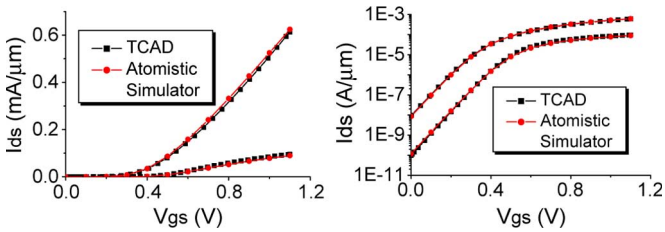

Fig. 2. Calibration of "atomistic" simulator on nominal-device TCAD data.

with density-gradient (DG) quantum corrections. The simulator was adjusted to match accurately the carefully calibrated TCAD device-simulation results provided by STMicroelectronics by adjusting the effective mass parameters involved in DG formalism and the mobility-model parameters. The calibration results are shown in Fig. 2, where "low" and "high" drain bias stand for 50 mV and 1.1 V, respectively. The following three major sources of statistical variability are investigated: random discrete dopants (RDD), LER, and polygate granularity (PGG). In simulation, the RDD are generated from continuous doping profile by placing dopant atoms on silicon-lattice sites within the device S/D and channel regions with a probability determined by the local ratio between dopant and silicon atom concentration. Since the basis of the silicon lattice is 0.543 nm, a fine mesh of 0.5 nm is used to ensure a high resolution of dopant atoms. However, without considering quantum–mechanical confinement in the potential well, in classic simulation, such fine mesh leads to carrier trapping at the sharply resolved Coulomb potential wells generated by the ionized RDD. In order to remove this artifact, the DG approach is employed as a quantum-correction technology for both electrons and holes [11]. The LER is introduced through 1-D Fourier synthesis, and random gate edges are generated from a power spectrum corresponding to a Gaussian autocorrelation function [12], with correlation length $\Lambda = 30$ nm and rms amplitude $\Delta = 1.3$ nm, which is the level that is achieved with current-lithography system [13]. The procedure used for simulating PGG involves the random generation of polycrystalline silicon grains for the whole gate region [10]. A large AFM image of polycrystalline silicon grains (Fig. 3) has been used as a template, and the image is scaled according to the experimentally observed average grain diameter through X-ray-diffraction measurements made both in $\theta - 2\theta$ and θ scan modes [14] (the average grain diameter is 65 nm). Then,

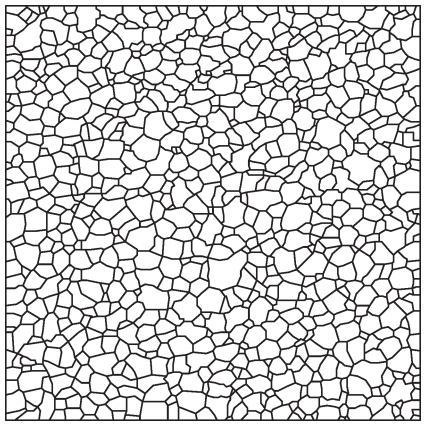

Fig. 3. Image of grain boundaries extracted from an AFM image of polysilicon grains.

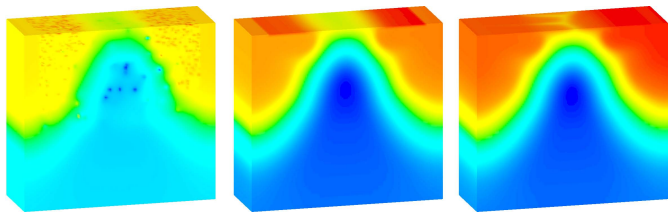

Fig. 4. Typical potential distributions corresponding to individual IPF source. From left to right, illustrations show the effect of RDD, LER, and PGG.

the simulator imports a random section of the grain template image that corresponds to the gate dimension of the simulated device, and along grain boundaries, the applied gate potential in the polysilicon is modified in a way that the Fermi level remains pinned at a certain position in the silicon bandgap. In the worst case scenario, the Fermi level is pinned in the middle of the silicon gap. However, precise quantification of gate contribution to the global statistical variability requires a more precise evaluation of Fermi-level pinning position. This is the reason why three sets of simulations with different pinning positions at the midgap, 200 mV, and 400 mV above midgap were carried out. The impact of polysilicon grain-boundary variation on device characteristics is simulated through the pinning of the potential in the polygate along the grain boundaries.

III. Results and Discussion

For each individual source of variability, 3-D simulations of 200 statistically different MOSFETs were carried out in order to extract the threshold-voltage variation. The typical potential distributions corresponding to each one of the simulated three sources of intrinsic parameter fluctuations (IPF) are shown in Fig. 4. The results from the simulation are shown in Fig. 5 and Table I. If we assume that the different variability sources are statistically independent, the final standard deviation of threshold-voltage variation for the combined effect of the three sources can be approximated by

$$\sigma V_T = \sqrt{\sigma V_{T1}^2 + \sigma V_{T2}^2 + \cdots + \sigma V_{Tn}^2} \tag{1}$$

where $\sigma V_{T1}, \sigma V_{T2}, \ldots, \sigma V_{Tn}$ are the standard deviations of threshold voltage resulted from individual variability sources.

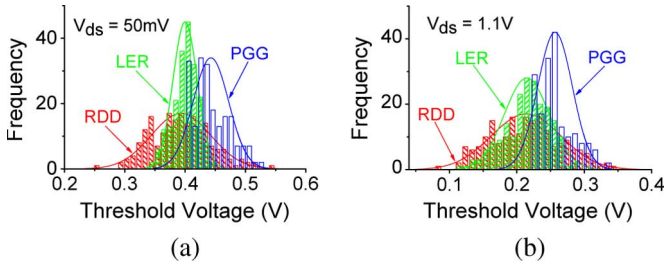

Fig. 5. Threshold-voltage distribution due to RDD, LER, and PGG. (a) $V_{\rm ds} = 50$ mV. (b) $V_{\rm ds} = 1.1$ V, while for PGG, the Fermi pinning potential is 200 mV above midgap.

TABLE I
SUMMARY OF SIMULATION RESULTS OF INDIVIDUAL IPF SOURCE, WHERE PGG[1], PGG[2], AND PGG[3] REPRESENT FERMI PINNING POTENTIAL AT MIDGAP, 200 mV, AND 400 mV ABOVE MIDGAP, RESPECTIVELY

	Vds (V)	Mean (V)	Standard deviation (V)	Max (V)	Min (V)
RDD	0.05	0.39	0.050	0.55	0.25
	1.1	0.21	0.052	0.34	0.083
LER	0.05	0.40	0.020	0.44	0.34
	1.1	0.21	0.033	0.29	0.12
PGG [1]	0.05	0.47	0.056	0.63	0.40
	1.1	0.28	0.046	0.42	0.22
PGG [2]	0.05	0.44	0.030	0.53	0.40
	1.1	0.26	0.026	0.34	0.22
PGG [3]	0.05	0.42	0.010	0.45	0.40
	1.1	0.24	0.010	0.26	0.22

The combined effects of RDD, LER, and PPG with midgap Fermi-level pinning from Table I would result according to (1) in $\sigma V_T \approx 78$ mV at $V_{\rm ds}$ of 50 mV, and $\sigma V_T \approx 77$ mV at $V_{\rm ds}$ of 1.1 V.

In order to verify the assumption for statistical independence of the variability sources, we carried out the statistical device simulation with all important variability sources (RDF, LER, and PGG) turned on simultaneously. The results are $\sigma V_T \approx 78$ mV at $V_{\rm ds}$ of 50 mV, and $\sigma V_T \approx 79$ mV at $V_{\rm ds}$ of 1.1 V, which indicates that the different intrinsic parameter fluctuations sources are indeed statistically independent, and the statistical addition of the individual variances is justified (this could greatly simplify the variability analysis of future devices).

These results have to be compared to the experimental results that show, as global dispersion, $\sigma V_T \approx 62$ mV at $V_{\rm ds}$ of 50 mV, and $\sigma V_T \approx 69$ mV at $V_{\rm ds}$ of 1.1 V. This indicates that the Fermi level is pinned above the midgap. Indeed, based on Table I, when pinning is considered at 200 mV above midgap, the summation of simulated individual contributions ($\sigma V_T \approx 62$ mV at $V_{\rm ds}$ of 50 mV, and $\sigma V_T \approx 67$ mV at $V_{\rm ds}$ of 1.1 V) becomes pretty close to the measured variability. Following [9], this Fermi-level pinning indicates a trap density equal to $1.5 * 10^{14}/\text{cm}^2$, which is a realistic value [15], [16].

IV. CONCLUSION

Owing to experimental local statistical variability measurements on a 45-nm LP technology platform N-MOSFET and atomistic simulations conducted for the same fully calibrated device, the impact of RDD, LER, and PGG are quantified in simulation, and the measurements result is consistent with global-simulation result. Concerning polygate contribution, the efforts were focused on the evaluation of the energy position of the Fermi-level pining at the grain boundaries. The simulation results indicate that RDD are still the dominant source of statistical variability (≈65%), while the influence of PGG (≈24%) is strongly dependent on the Fermi-level pinning position, which in turn indicates strong processing dependence. It is worth noting that similar methodology could be applied to estimate the metal-granularity contribution to local statistical variability due to work-function fluctuation through the gate area.

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