Monte Carlo Study of Coupled SO Phonon-Plasmon Scattering in Si MOSFETs with High $\kappa$-Dielectric Gate Stacks: Hot Electron and Disorder Effects

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Summary. A Monte Carlo scheme is described for simulating electron-phonon-plasmon scattering in realistic high-$\kappa$ gate stack Si MOSFETs that accounts for hot electron effects, modulation of the electron-phonon-plasmon scattering rates by the interface boundary roughness and inhomogeneity of the dielectric layers.

1 Introduction

There is strong industrial interest in implementing high-$\kappa$ gate stacks with metal gates into decanano silicon MOSFET technology to allow physically thicker dielectrics in order to reduce the gate leakage (tunnelling) current prevalent in ultra-thin silicon dioxide in present Si MOSFETs. However, it has been pointed out [i, ii] that severe mobility degradation ensues because of the strong coupling of carriers in the channel to soft, surface optical (SO) phonons [iii, iv] in the vicinity of the high-$\kappa$ dielectric interface. Recently, we have shown [ii] that for ideal interfaces and homogeneous dielectrics it might be possible to offset the mobility degradation by a mobility enhancement that derives from using a strained silicon channel. Unfortunately, the electron-phonon-plasmon scattering in such structures is a complex process that involves the entire gate stack via the coupling of plasmons in the gate and substrate to the phonon modes. Because the renormalised phonon/plasmon energies and screening are sensitive to layer thicknesses the electron-phonon-plasmon scattering strength is modulated by the roughness of the interfaces.
Both the gate-dielectric interface and the dielectric/interfacial layer-semiconductor interfaces will contribute to remote surface roughness effects. In addition there is evidence that many of the high-\(\kappa\) gate stacks display significant phase separation that will distort our assessment of the spatial dependence of the scattering rates (Fig. 1). An understanding of the coupling problem also requires an evaluation of the effects of the variation of the carrier velocity dispersion (via electron temperature) between source and drain that acts to modulate the Landau damping of the coupled system.

Fig. 1. (a) Features of realistic high-\(\kappa\) gate stack MOSFETs – adapted from [v].
(b) Layer inhomogeneities at different cross sections in the stack.

2 Monte Carlo Scheme

We extend the formalism developed by Fischetti et al [i] to include an inhomogeneous dielectric, interfacial layer and surface roughness at the different interfaces. The solution domain is partitioned into vertical rectangular columns located by discrete coordinates \((X, Y)\) in the stack plane (see Fig. 2). Each column comprises blocks in which the material parameters are approximated as constant. Because of interface roughness and separated phases the blocks are disjoint. Each vertical column labelled by \((X, Y)\) is then treated as a slice through a stack of uniform layers from gate down to the channel. The screened SO phonon scattering rates for each column \(R(k, k'; X, Y)\) are then determined by the formalism in [1] assuming a bare channel plasmon energy \(\hbar \omega_p(X, Y)\) and local electron temperature \(T_e(X, Y)\) derived respectively from the averages of the electron density \(n(x, y)\) and temperature \(T_e(x, y)\) over the channel block at \((X, Y)\). Landau damping is computed from a hot electron Lindhard model.

The full Monte Carlo scheme proposed here is compute intensive. However, simplifications may be made by using Padé approximants for the plasma dispersion function following [vi]. Coarse-graining the column widths also significantly reduces the complexity. This procedure is a good
approximation for the mobility-degrading SO phonon scattering but fails to capture the elastic boundary scattering off the rough silicon channel to insulator interface. Boundary scattering is therefore treated by standard methods [vii]. The lowest order simulation uses a single column with averaged interfacial layer dimensions and parameters to form the stack blocks.

3 Polycrystallinity and Intrinsic Parameter Fluctuations

Preliminary results show that strong parameter fluctuations in nano-scale MOSFETs are introduced by non-uniformity of the dielectric properties of the high-κ material due to random grain orientation (polycrystalline HfO₂ with different orientations of grains resulting in varying dielectric properties) and phase separation (HfO₂ crystallised in ‘islands’ within an amorphous SiO₂ matrix). Such variations in the film structure are shown in Fig. 2a, which shows a plan-view TEM image of a HfSiO film, with phase separation. A 2D Fourier-Fractal model is shown in Fig. 2b.

![Fig. 2a. Plan-view TEM image of a HfSiO film illustrating phase separation of the Hf and Si oxides.](image)

![Fig. 2b. Stochastic dielectric pattern from 2-D Fourier-Fractal synthesis](image)

The structural fluctuations in the dielectric of the oxide lead to corresponding fluctuations in the surface potential as illustrated in Fig. 3a. The particular random dielectric pattern in this particular case is shown in the plane above the device. The regions of high dielectric producing higher surface potentials, leading to fluctuations in the threshold voltage of nano-scale devices as can be seen from Fig. 3b, where we show the $I_D-V_G$ characteristics for ten 50×50 nm MOSFETs clearly demonstrating the spread in threshold voltages, modelled using Drift Diffusion. Also shown are the curves for a pure SiO₂ gate oxide and pure high-κ (above an interfacial layer) the limiting cases for the fluctuations. In all cases the physical gate oxide is 4 nm thick and degradation in subthreshold slope due to the reduced gate oxide capacitance when SiO₂ is employed is evident.
Fig. 3a. Electrostatic potential in a 50×50 nm MOSFET showing the fluctuations in surface potential due to the spatial variations in gate dielectric, shown in the plane above.

Fig. 3b. $I_D V_G$ characteristics for 10 devices with random dielectric pattern, and the limiting cases.

4 Interfacial Oxide Layer

We find that the rough interface boundaries give rise to a random variation of the effective dielectric thickness that carries through into a modulation of the electron-phonon-plasmon coupling and local phonon energies. This is illustrated by a simple single-column Monte Carlo simulation for a gate stack consisting of a HfO$_2$ high-$\kappa$ and a SiO$_2$ interfacial layer, similar to that illustrated in Fig 1. Fig. 4 shows the variation in computed mobility versus oxide interfacial layer thickness with a constant inversion layer field of 1MV/cm.

Fig. 4. Effective mobility within the channel as a function of the interfacial (SiO$_2$) layer thickness.
5 Electron temperature

Electron heating at various locations in the device severely alters the influence of Landau damping on the plasmon modes. The variation of electron temperature along the channel thus provides an additional spatial modulation of the scattering rates and quanta. The typical variation of $T_e$ is shown in Fig. 5 showing the Monte Carlo computed electron temperature for a degenerate channel in a 67nm effective channel length Si n-MOSFET [8].

![Figure 5](image_url)

Fig. 5. Variation in electron temperature along channel for degenerate electrons in a Si n-MOSFET. $V_G=V_D=IV$. Vertical dashed lines indicate the start and end of the metallurgical gate.

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7 References