Simulation of statistical variability in 18 and 13nm bulk MOSFETs

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Summary

Well-scaled bulk MOSFETs with 18 and 13nm gate lengths, representative of the 16nm technology generation, have been designed using TCAD process simulation. The statistical variability due to random discrete dopants (RDD) and line edge roughness (LER) has been evaluated using full-scale 3D device simulation and statistical compact models are being extracted in order to design future variability-resistant circuits and systems.

At the 32nm technology generation, statistical variability has become a serious problem for scaling and the design of corresponding circuits and systems. At, and beyond, the 22nm technology generation statistical variability in bulk MOSFETs will be severe. Addressing this issue, and investigating possible alternative architectures in memory design, is the goal of the European FP7 project TRAMS in which Glasgow University is a partner with Universitat Politècnica de Catalunya, IMEC and Intel. Within the project, Glasgow is responsible for the design of a range of devices considered in TRAMS, their statistical simulations [1] and the extraction of nominal and statistical compact models.

The first types of investigated devices are bulk MOSFETS at the 16nm technology generation and beyond. To this end we have designed well-scaled bulk MOSFETs with 18nm and 13nm channel lengths. The device design was performed using a commercial TCAD simulator and the resultant n-channel device structures are illustrated in Fig. 1.

The doping profiles obtained from the process simulation are transferred to the Glasgow ‘atomistic’ device simulator, which is then calibrated to match the I-V characteristics obtained from the TCAD simulations. The \( I_D-V_G \) characteristics for the uniform devices are shown in Fig. 2. The Glasgow simulator is an advanced 3D drift-diffusion simulator tailored specifically for variability simulations. It includes density gradient quantum corrections for electrons and holes that allow the accurate resolution of every discrete dopant in the simulation charges.

We have simulated \( I_D-V_G \) characteristics for ensembles of 200 devices that are unique in their random distribution of discrete dopants and in gate LER. We also investigate degradation effects on reliability [2]. From the characteristics, statistical compact models are extracted that can be used by project partners to investigate the effects of variability on circuits and systems. We will present comprehensive analysis of the statistical variability in the 18 and 13 nm devices.


Fig. 1. 18 and 13nm bulk MOSFET structures from TCAD process simulation.

Fig 2. \( I_D-V_G \) characteristics for the 18 and 13nm uniform devices with no variability.

Fig. 3. Electrostatic potential in an 18nm MOSFET with RDD and LER. Conduction band edge is shown above.

Fig. 4. \( I_D-V_G \) characteristics for the 18nm device. 200 transistors with RDD and LER are simulated at 1V drain bias. Inset shows the corresponding \( V_T \) distribution.